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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,925	07/07/2003	Takahiro Kawano	239801US2	6929

22850 7590 10/24/2007
OBLON, SPIVAK, MCCLELLAND MAIER & NEUSTADT, P.C.
1940 DUKE STREET
ALEXANDRIA, VA 22314

EXAMINER

NADAV, ORI

ART UNIT	PAPER NUMBER
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2811

NOTIFICATION DATE	DELIVERY MODE
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10/24/2007

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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<p align="center">Office Action Summary</p>	<p>Application No.</p> <p align="center">10/612,925</p>	<p>Applicant(s)</p> <p align="center">KAWANO ET AL.</p>	
	<p>Examiner</p> <p align="center">Ori Nadav</p>	<p>Art Unit</p> <p align="center">2811</p>	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
 - If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
 - Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 October 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,2,4-7,9,17,19-21,23-25,27,35,37-39,41 and 43-51 is/are pending in the application.
- 4a) Of the above claim(s) 2,7,9,17,19,20,25,27,35,37,38 and 48-51 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-6,21,23,24,39,41 and 43-47 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
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| <p>1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)</p> <p>2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)</p> <p>3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)</p> <p>Paper No(s)/Mail Date _____</p> | <p>4) <input type="checkbox"/> Interview Summary (PTO-413)</p> <p>Paper No(s)/Mail Date. _____</p> <p>5) <input type="checkbox"/> Notice of Informal Patent Application</p> <p>6) <input type="checkbox"/> Other: _____</p> |
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DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 4-6, 21, 23-24, 39, 41 and 43-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nagata et al. (6,316,814) in view of Merrill et al. (6,606,120) and Applicant Admitted Prior Art (AAPA).

Nagata et al. teach in figure 1A and related text a semiconductor device comprising:

a semiconductor layer which includes a first semiconductor region 11 of a first conductivity type, and a plurality of second semiconductor regions 20 of the first conductivity type formed on the first semiconductor base region,

and a plurality of second semiconductor regions 20 of the first conductivity type;

a gate wiring 13 which is formed on the semiconductor layer via a first insulating film 16;

a plurality of main electrodes 15A (or the electrode located just below line 15A, see also figure 1B) which are electrically connected to the plurality of second semiconductor regions and which are insulated from the gate wiring, wherein the gate wiring is arranged between the main electrodes;

a second insulating film 24 which is formed on an upper surface of the gate wiring; and

upper surfaces of the main electrodes are higher than the highest portion of an uppermost surface of the gate wiring.

Nagata et al. do not teach a base region of a second conductivity type formed above the first semiconductor region and a connecting plate which is connected to a lead frame and is directly connected onto the upper surfaces of the main electrodes.

Merrill et al. teach in figure 1A and related text forming an imaging device in a triple well, i.e. forming an imaging device in a semiconductor layer which includes a first semiconductor region of a first conductivity type and a base region of a second conductivity type formed above the first semiconductor region.

AAPA teaches in figure 21 and related text (page 3, lines 9-10) a connecting plate 2109 is directly connected onto the upper surfaces of the main electrodes of the device 2105.

AAPA further teaches in figure 20 and related text a wiring 2004 is directly connected between the main electrodes of the device 2002 and the lead frame 2003. AAPA also teaches that the connecting plate replaces the wiring connecting the main electrodes of the device and the lead frame.

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form Nagata et al.'s device in a triple well and to use a lead frame in Nagata et al.'s device and to connect a connecting plate directly between the upper surfaces of the electrodes and the lead frame in Nagata et al.'s device, in order to improve the device characteristics by providing better electrical isolation for the device,

and in order to operate the device in its intended use (by providing lead frame and external connections) and to reduce the contact resistance of the device by using a connecting plate between the electrodes and the lead frame, respectively.

The combination is motivated by the teachings of Merrill et al. which points out the advantages of using a triple well (column 2, lines 46-50).

The combination is also motivated by the teachings of AAPA which points out the advantages of using a connecting plate instead of external wiring.

Regarding the claimed limitations of main electrodes being in contact with a contact region of the connecting plates and in an area under the contact region of the connecting plates the upper surfaces of the main electrodes are higher than the highest portion of an upper surface of the gate wiring, these features are inherent in prior art's device because the main electrodes are connected to the connecting plates and they thus must be in contact with a contact region of the connecting plates. The area under the contact region of the connecting plates must be where the upper surfaces of the main electrodes are higher than the highest portion of an upper surface of the gate wiring, because the contact region must be located above the upper surfaces of the main electrodes.

Note that forming Nagata et al.'s device in a triple well, means that the device comprises a semiconductor layer which includes a first semiconductor region of a first conductivity type, and a base region of a second conductivity type formed above the first semiconductor region, as claimed.

Regarding claims 4, 21, 23, 39, 41 and 44, AAPA teaches gate wiring 2107 comprising aluminum. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form the main electrodes and the connecting plate of a plurality of metal layers comprising aluminum in Nagata et al.'s device in order to reduce the contact resistance between the main electrodes and the lead frame.

Regarding claims 4 and 46, Nagata et al. teach a second insulating film 24 extends between plurality of metal layers, and under the main electrode.

Regarding claim 5, Nagata et al. teach in figure 1 plurality of main electrodes are formed apart from the gate wiring with a gap there between.

Regarding the process limitations recited in claims 23 and 41 ("the first connecting plate is connected to the first main electrode and the second main electrode by ultrasonic bonding") these would not carry patentable weight in this claim drawn to a structure, because distinct structure is not necessarily produced.

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Brown*, 173 USPQ 685; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by

process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that the applicant has the burden of proof in such cases, as the above case law makes clear.

Regarding claims 6, 24 and 43, Nagata et al. teach a first gate electrode which is formed in the cell forming region and controls continuity between the first semiconductor region and the second semiconductor region; and first and second main electrodes (see the array in figure 1B) which are electrically connected to the plurality of second semiconductor regions respectively and which are formed at predetermined intervals in the cell forming region on the semiconductor layer.

Regarding claim 24, Nagata et al. do not teach a first semiconductor layer of a first conductivity type. It would have been obvious to a person of ordinary skill in the art at the time the invention was made to form a first semiconductor layer of a first conductivity type in Nagata et al.'s device in order to improve the electrical isolation of the device.

Regarding claims 43, 45 and 47, the claimed limitations of main electrodes comprise a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, wherein the second main electrode is thicker than the first main electrode layer, these features are inherent in prior art's device, because the first main

electrode layer is not necessarily distinguishable from the second main electrode layer. Thus, the main electrodes of prior art's device can be arbitrarily divided into a first main electrode layer and a second main electrode layer which is formed on the first main electrode layer, wherein the second main electrode is thicker than the first main electrode layer, as claimed.

Response to Arguments

Applicant's arguments with respect to claims 1, 4-6, 21, 23-24, 39, 41 and 43-47 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ori Nadav whose telephone number is 571-272-1660. The examiner can normally be reached between the hours of 7 AM to 4 PM (Eastern Standard Time) Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Gurley can be reached on 571-272-4670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



O.N.
10/18/07

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